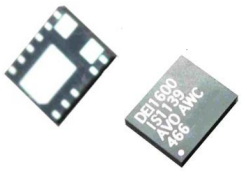
Device Engineering Incorporated

385 East Alamo Drive
Chandler, AZ 85225
Phone: (480) 303-0822
Fax: (480) 303-0824
E-mail: admin@deiaz.com

Preliminary Information

DEI1600
SURGE BLOCKING MODULE (SBM)

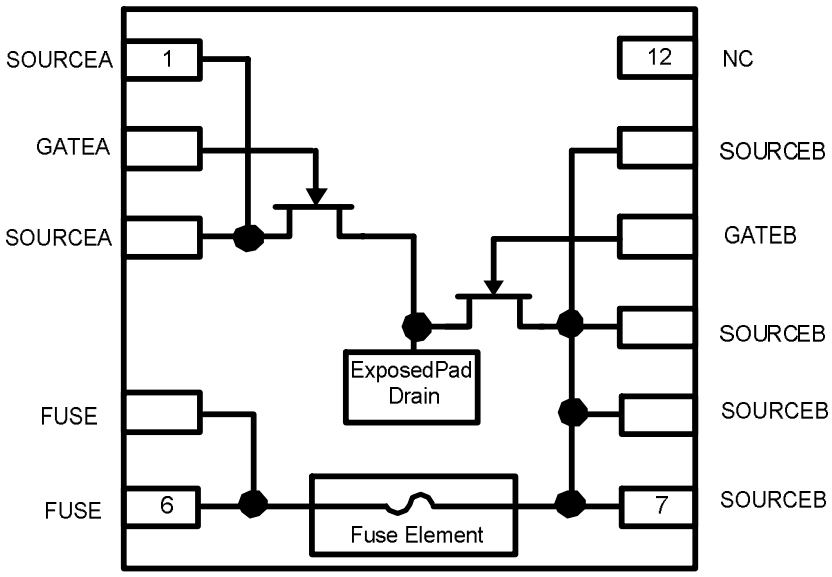
FEATURES



- 1600V bidirectional surge current limiter with integral 115VAC fuse element.
- Circuit protection for A350 XWB lighting environment pin injection waveforms (Voc/Isc):
  - Waveform 5A: 1500V/15A, 500V/500A, 300V/300A, 200V/200A, 100V/100A
  - Waveform 3: 1500V/60A, 600V/24A, 250V/10A, 100V/4A (1 & 10MHZ)
  - Waveform 2: 1600V/107A, 750V/50A, 250V/10A, 100V/4A
  - Multiple Stroke, Multiple Burst
- Low JFET series resistance: 1.7Ω at +85°C
- Operating currents: ±0.45A
- Package: 12L DFN 6x7.7
- -40°C to +85°C temperature range

PIN ASSIGNMENTS

Top View



Note: The exposed pad is electrically connected to the internal node shown.
It should be soldered to an electrically isolated PCB land to provide a thermal heat sink

Figure 1: 12L DFN Pinout

GENERAL DESCRIPTION

OVERVIEW

The DEI1600 Surge Blocking Module (SBM) is a high voltage, bidirectional current limiting element implemented with normally ON N-Channel Silicon Carbide JFET technology. The device is intended to be used in conjunction with a Transient Voltage Suppressor (TVS) diode to implement a current limiting / voltage clamping protection network. It is designed to limit surge current during, and withstand the stress of lighting induced transients in aircraft. It is intended for equipment required to operate without damage in the presence of the following pin injection damage waveforms as defined in ABD0100.1.2G.

- Waveform 5A: 1500V/15A, 500V/500A, 300V/300A, 200V/200A, 100V/100A
- Waveform 3: 1500V/60A, 600V/24A, 250V/10A, 100V/4A (1 & 10MHZ)
- Waveform 2: 1600V/107A, 750V/50A, 250V/10A, 100V/4A
- Multiple Stroke, Multiple Burst

In normal operation, the SBM acts as a low value series resistor (< 1.7Ω for JFETs) and is designed to operate at currents up to ±0.45A. In surge stress operation, the TVS device conducts surge current when the surge voltage exceeds the TVS standoff voltage. The series SBM limits the surge current to a few Amps, thus allowing use of small, low power, low capacitance TVS diodes to provide the voltage clamp protection.

An integral fuse element, when connected as shown in **Figure 2**, provides "Fail Safe" operation during faults such as inadvertent application of aircraft power. The fuse element is designed to remain intact for the specified lightning surges. However sustained faults, such as the application of aircraft power (28VDC or 115VAC), induce sufficient current to open the fuse and block the fault. The fuse controlled "limited let-through energy" prevents damage to the PCB and aircraft wiring. The TVS is selected to withstand the let-through energy, hence the downstream circuitry is protected from damage. To restore normal operation, the fault must be cleared and the SBM replaced.

Figure 3 depicts an application with 230VAC fault protection. The integral 115V fuse is not used, and is replaced by a fuse external to the SBM. The external fuse element is selected with suitable voltage/current rating to withstand the lightning surge current without fusing, but open and block 230VAC faults before damage occurs to the wiring, PCB, and TVS.

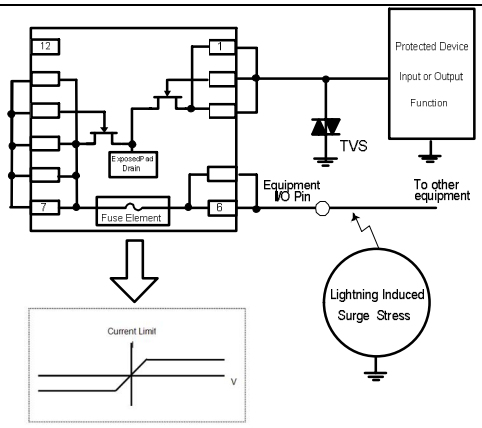


Figure 2: Application Circuit using Integral 115VAC Fuse

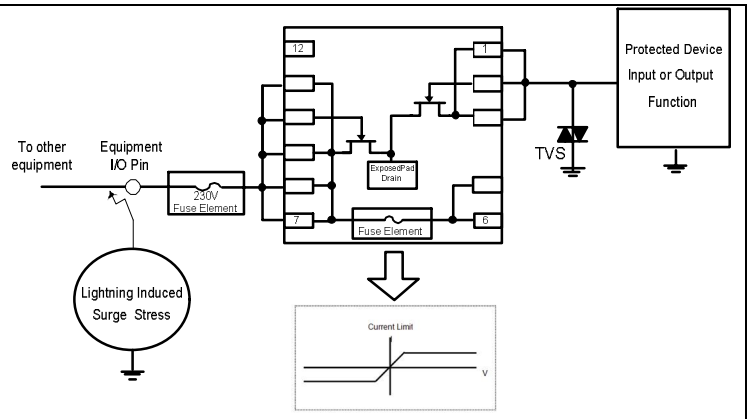


Figure 3: Application Circuit using External 230VAC Fuse

CURRENT LIMITING

The figures below illustrate SBM current limiting for several surge conditions. These (simulated) waveforms result when the indicated stress voltage waveform is applied directly across the SBM limiter.

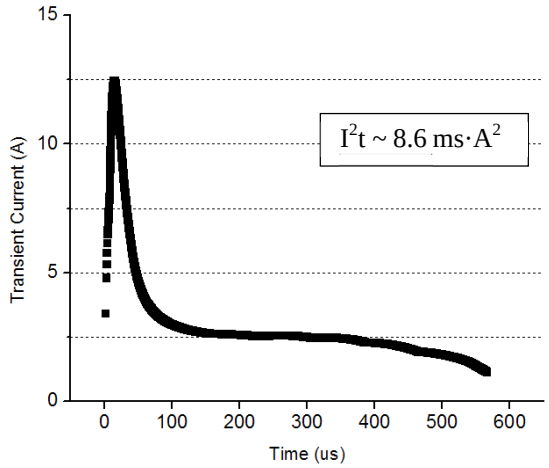


Figure 4: SBM Limit Current – DO-160 WF5A 1500V/15A

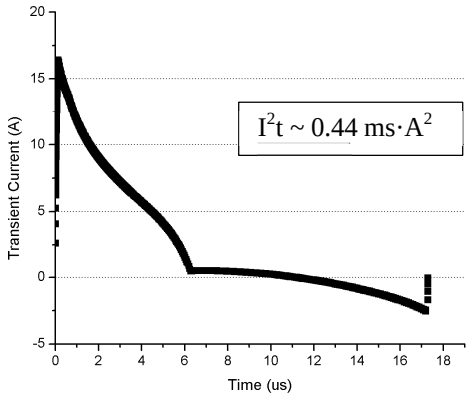


Figure 5: SBM Limit Current – DO-160 WF2 1600V/107A

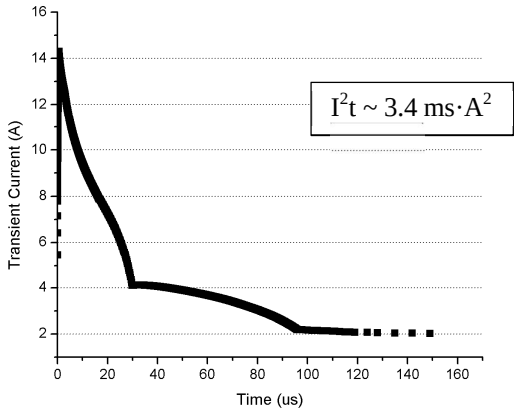


Figure 6: SBM Limit Current – DO-160 WF4 1600V/106A

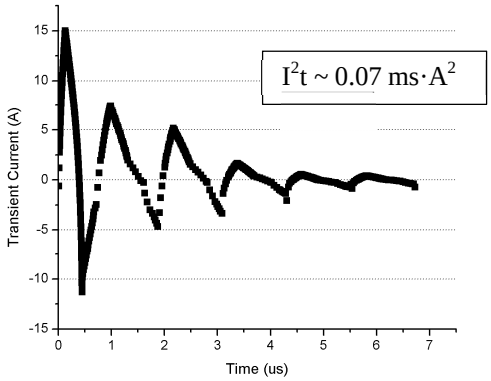


Figure 7: SBM Limit Current – DO-160 WF3 1MHz 1500V/60A

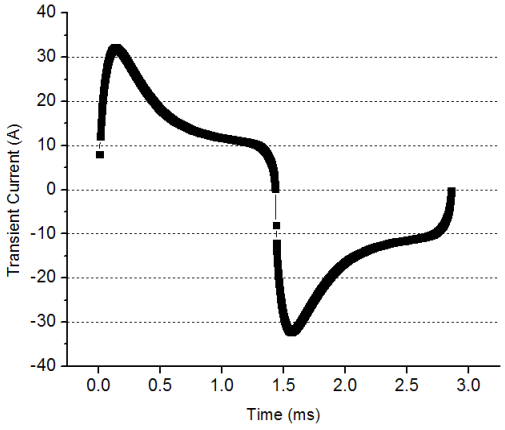


Figure 8: SBM Limit Current - 115VAC, 800Hz

The table below contains observed characteristics of the surge limited current pulse that is produced when the specified waveform is applied directly across the SBM (no TVS). The I^2t value is useful in evaluating fuse characteristics and calculation of the energy dissipated in series resistive elements. The I_{AVE} and t_W values are useful in calculation of TVS pulse power.

Table 1 SBM Surge Current Characteristics

Surge Waveform	Effective Heating Current I^2t ($ms \cdot A^2$)	Average Current I_{AVE} (A)	Pulse Width t_W (us)	Energy Dissipated in SBM E_D (mJ)
WF5A 1500V / 15A	6.0	1.1	1000	425
WF5A 500V / 500A	14.3	2.9	1000	368
WF5A 300V / 300A	10.3	2.9	1000	276
WF5A 200V / 200A	15.7	3.1	1000	250
WF5A 100V / 100A	26.1	3.2	1000	144
WF3 1500V / 60A 1MHz		tbd …		
WF3 600V / 24A 1MHz				
WF3 250V / 10A 1MHz				
WF3 100V / 4A 1MHz				
WF3 1500V / 60A 10MHz				
WF3 600V / 24A 10MHz				
WF3 250V / 10A 10MHz				
WF3 100V / 4A 10MHz				
WF2 1600V / 107A				
WF2 750V / 50A				
WF2 250V / 10A				
WF2 100V / 4A				

Note:
Values are from limited characterization data. One lot, 10 pcs, highest values recorded.

INTEGRATED 115VAC FUSE

A fuse's "melting I^2t" (aka "pre-arc I^2t") parameter defines the current-time relationship at which the fuse will open. The SBM's melting I^2t value is ~80 ms·A^2 for short pulses (10 to 100s us). This is higher than the maximum I^2t of the SBM's surge current produced during the specified lightning stress waveforms (Refer to Table 1). Thus the fuse remains intact during lighting stress events.

The fuse is selected to melt (open) as quickly as possible upon inadvertent application of aircraft power (115VAC/400Hz) in order to minimize the "let-through current" and thereby prevent damage to the wiring and PCB. Application of 115V/400Hz develops sufficient I^2t to melt the fuse within two cycles. The open fuse will block 115Vac±10% / 350-800Hz.

Figure 9 illustrates the joule integral relationship between the integral fuse element and the surge currents and the 115VAC fault current. The y-axis I^2t units are ms·A^2, and therefore proportional to the resistive heating of the fuse element. The "DEI1600 Fuse" curve denotes the current-time that will cause the fuse element to arc (open). The "Transient WFM Envelope" denotes the range of the JFET limited current that will flow during WF5A lightning transients; WF5A is the worst case (highest I^2t) waveform. The "115VAC Envelope" denotes the range of JFET limited current that will flow during inadvertent application of 115VAC 400Hz. The "Fuse Trigger" region indicates the range of fuse "pre-arcing" time when 115VAC is applied.

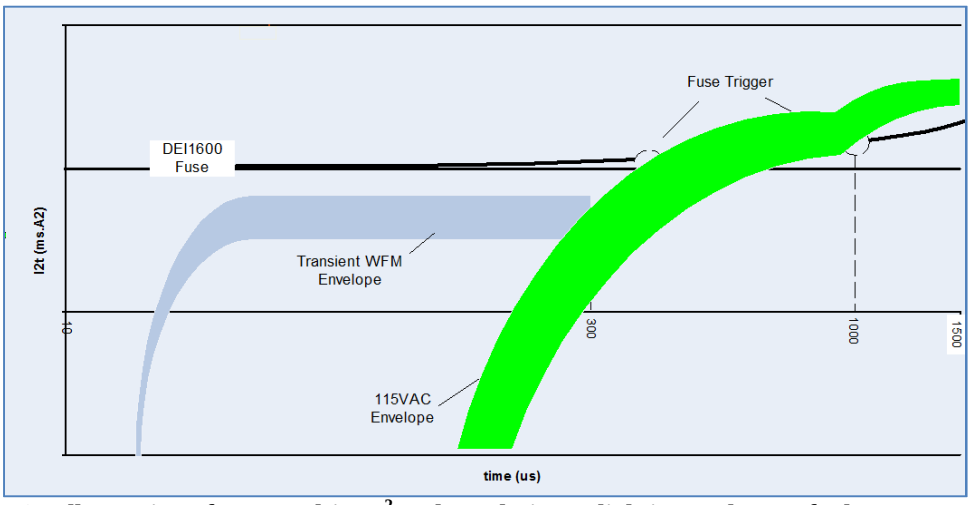


Figure 9: Illustration of Fuse melting I^2t value relative to lighting and 115V fault current values

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Table 2: Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Storage Temperature	$T_{STORE-MAX}$	-65	+150	°C
Junction Temperature, Continuous Operation	T_{OP-MAX}	-40	+145	°C
Source to Source Surge Voltage Gate to Source Voltage (A or B) Gate to Drain (Exposed Pad) Surge Voltage	V_{MAX}	 -17 -1600	±1600 +5 +5	V

RECOMMENDED OPERATING CONDITIONS

Table 3: Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Ambient Operating Temperature	T_{OP}	-40	+85	°C
Operating Voltage (SourceA to SourceB)	V_{DIF}	-0.77	+0.77	V
Gate to Source Voltage (A or B)	V_{GS}	0	0	V
Operating Current	I_{OP}	-0.45	+0.45	A

DC CHARACTERISTICS

Table 4: DC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
JFET CHARACTERISTICS						
Operating Resistance SourceA to SourceB (Both JFETs)	R_{ON-SBM}	I_{SS} = -0.45A to +0.45A Each Gate-Source shorted T_A = -40°C /2 T_A = 25°C /1 T_A = 85°C /2 T_A = 125°C /2	 - - 	 0.63 0.82 1.2 tbd	 1.0 1.3 1.7 	Ω
JFET ON Resistance, R_{DSon} (each JFET)	$R_{ON-JFET}$	I_{DS} = +0.45A Gate-Source shorted T_A = -40°C /2 T_A = 25°C /1 T_A = 85°C /2 T_A = 125°C /2	 	 0.31 0.39 0.52 tbd	 0.58 	Ω
Drain to Source Blocking Voltage (Each JFET)	BV_{DS}	I_D = 600µA V_G = -15V /3 T_A = 25°C	 1700 	 - 	 - 	V
Drain Saturation Current (Each JFET)	ID_{SAT}	V_{DS} = 4V, 450us pulse Gate-Source shorted T_A = -40°C /2 T_A = 25°C /1 T_A = 85°C /2 T_A = 125°C /2	 	 7.2 6.3 5.3 tbd	 10 	A
Drain Leakage Current (Each JFET)	ID_{OFF}	V_{DS} = 1100V, 450us pulse V_{GS} = -15V T_A = -40°C /2 T_A = 25°C /1 T_A = 85°C /2 T_A = 125°C /2	 	 5.3 6.5 11.2 tbd	 250 	uA
FUSE CHARACTERISTICS						
Fuse Resistance, SourceB to FUSE	R_{FUSE}	I_T = 0.45A T_A = -40°C /2 T_A = 25°C /1 T_A = 85°C /2 T_A = 125°C /2	 	 52 62 69 TBD	 150 	mΩ
Rated Current	I_rated	Max Rated Current, Continuous Operation	-	1	-	A
Rated Voltage	V_rated	Continuous blocking voltage after fusing. 350-800Hz Vac	-	115	-	Vac

Notes:
1. 100% tested
2. Sample tested each lot
3. 100% tested at wafer probe
4. Guaranteed by design, not production tested

DYNAMIC CHARACTERISTICS

Table 5: Dynamic Characteristics (each JFET)

Conditions: T_A = +25 ºC unless otherwise noted						
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance Cgs + Cgd	Ciss	V_{GS} = -15V V_{DS} = 80V Test_Freq = 1MHz JESD24	-	142	-	pF
Output Capacitance Cgd + Cds	Coss		-	49	-	pF
Notes: 1. Dynamic characteristics are tested at wafer level.						

CHARACTERIZATION DATA

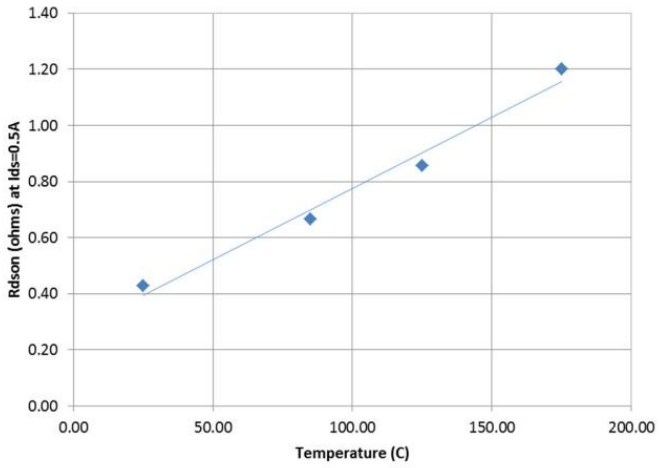


Figure 10: JFET $R_{DS\ ON}$ vs Temperature

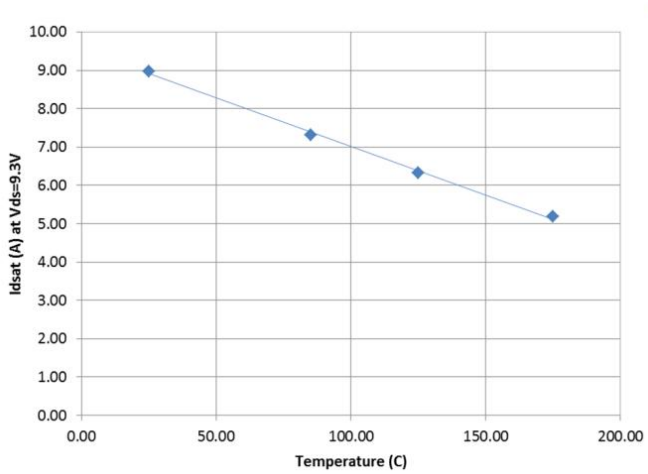


Figure 11: JFET I_{DSAT} vs Temperature

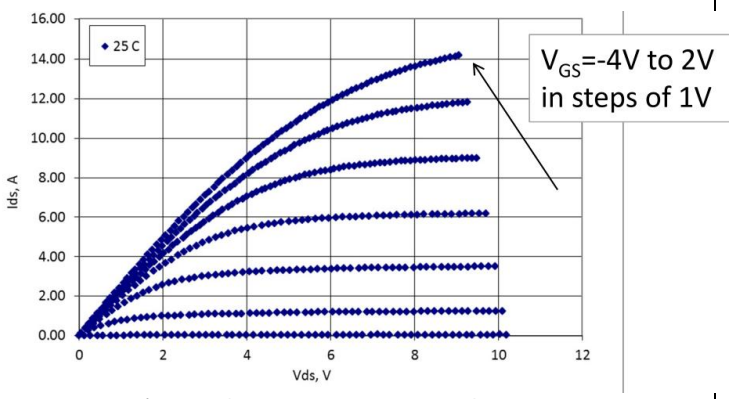


Figure 12 JFET I_{DSAT} vs V_{DS} Over V_{GS}

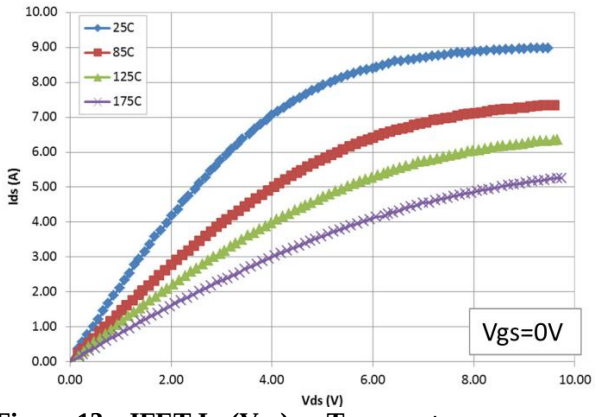


Figure 13: JFET $I_{DS}(V_{DS})$ vs Temperature

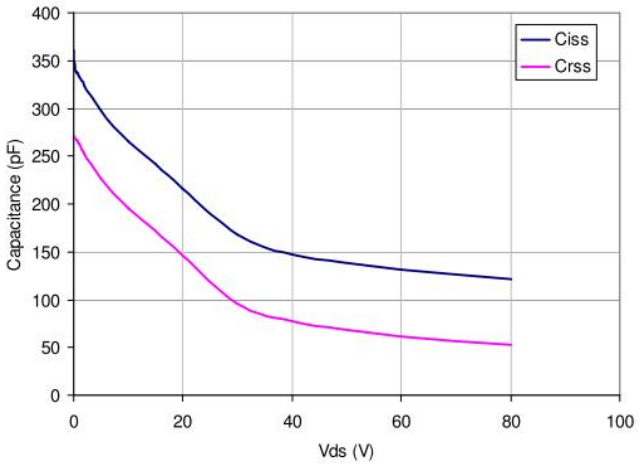


Figure 14: JFET Capacitance vs Vds (Vgs = -15V)

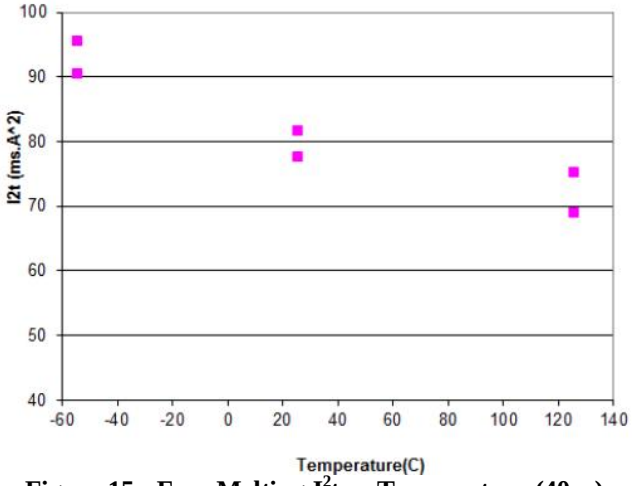


Figure 15: Fuse Melting I^2t vs Temperature (40us)

Impedance vs Frequency
TBD

APPLICATION INFORMATION

TVS SELECTION

The Transient Voltage Suppressor (TVS) should be selected with a power rating that can:

- Withstand the SBM limited lightning surge current without exceeding the TVS power rating.
- Withstand the SBM and fuse limited 115VAC and 28VDC fault current "let through energy" without an open-circuit failure of the TVS. As a fault event requires repair/replacement of the protection circuitry, it is permissible for the TVS to be overstressed, providing it continues to protect the downstream circuitry.

13V and 48V, 600W (TBC) TVSs have been evaluated and found to be suitable for the specified lightning waveforms and inadvertent faults.

SAFE OPERATING AREA (SOA)

Figure 16 describes the SBM static safe operating area at 85°C ambient temperature. At low voltages, the SOA is limited by the fuse element continuous current. At higher voltages, it is limited by package temperature which is influenced by the PCB thermal design.

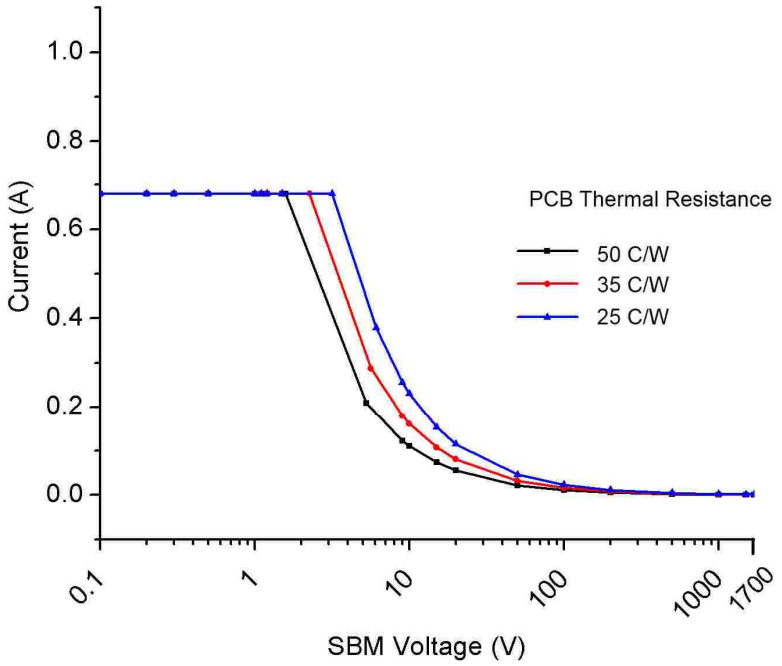


Figure 16: Static Safe Operating Area vs. Θ_{JA} (Ta = 85°C)

PCB DESIGN RECOMMENDATIONS

The 12DFN package incorporates a bottom thermal contact (BTC) and two smaller dummy contacts. The dummy contacts exist to balance the solder density to center the part during soldering. The thermal contact exists to conduct heat from the SBM to a heat spreader land on the PCB. The BTC is electrically connected to the JFET drains; thus the PCB heat spreader land must be electrically isolated. The BTC voltage will nearly reach the surge voltage in one polarity; hence the PCB clearance from the BTC must observe surge voltage design rules. The PCB should also minimize capacitive coupling to internal ground and power planes to minimize RF resonance during BCI stress.

To maximize the heat spreader performance, it is recommended the PCB design include thermal VIAs to heat spreader lands on the back side of the PCB, and on internal planes if possible. Depending on the soldering process, VIAs should be plugged or tented to prevent solder wicking, or partially filled by Hot Air Solder Leveling. The solder process should achieve a minimum of 50% BTC solder wetting. The solder attach must be free of solder balls, solder bulges, and contamination under the SBM in order to maintain clearance between BTCs/terminals required for high voltage operation.

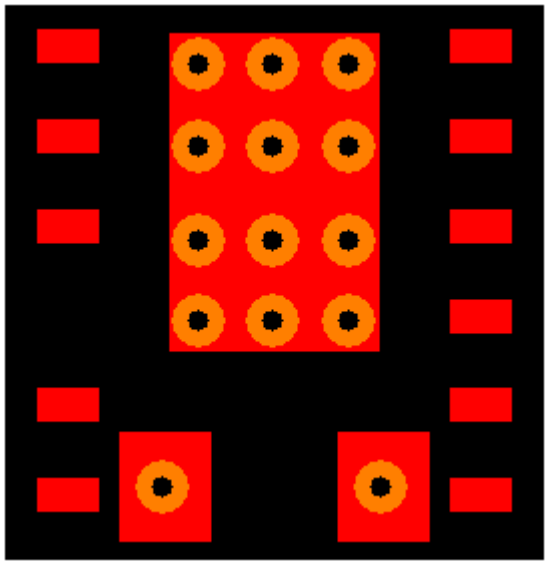


Figure 17: Example PCB footprint with thermal VIAs

ORDERING INFORMATION

Table 6 Ordering Information

Part Number	Marking	Package	Burn In	Temperature
DEI1600-MIS-G	DEI1600/ISYYWWe4	12DFN6x7.7	No	-40ºC to +85ºC

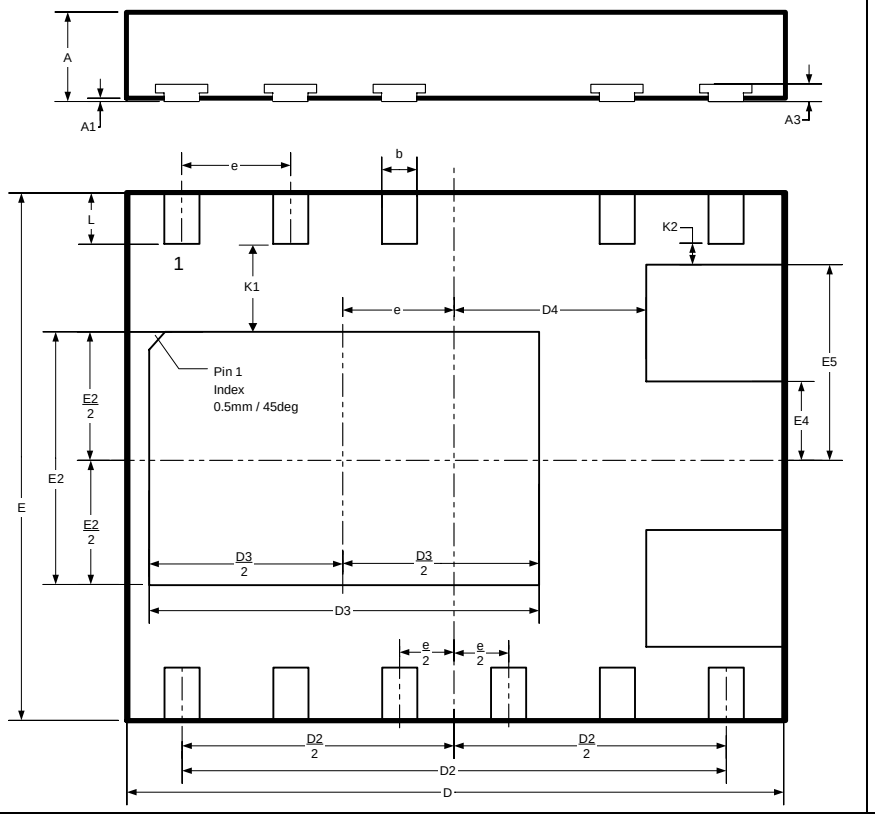
PACKAGE DESCRIPTION

Table 7 Package Characteristics

PACKAGE TYPE	THERMAL RESIST. (ºC/W)	JEDEC MOISTURE SENSITIVITY LEVEL & PEAK BODY TEMP	LEAD FINISH / JEDEC Pb-Free DESIGNATION	Pb Free Type
12L DFN 6x7.7	θ_{JC} ~3 θ_{JA} ~50 (1) θ_{JA} ~35 (2) θ_{JA} ~25 (3)	MSL 1 (TBC) 260ºC	NiPdAu e4	RoHS

Notes:

1. Single sided PCB. SBM soldered to thermal land.
2. Single sided PCB. Thermal land with 12 thermal VIAs.
3. 4 layer PCB. SBM soldered to thermal land with 12 thermal VIAs contacting heat spreader lands on all 4 layers



SYMBOL	MIN	NOM	MAX	NOTES
A	1.30	1.40	1.50	
A1	0.00	0.02	0.05	
A3		0.20		Ref
b	0.33	0.42	0.51	
D		7.69		BSC
D2		6.35		BSC
D3		4.55		BSC
D4	2.20	2.25	2.30	
E		6.15		BSC
e		1.270		BSC
E2	2.90	2.95	3.00	
E4	0.82	0.87	0.92	
E5	2.18	2.23	2.28	
K1	0.95	1.00	1.05	
K2	0.20	0.25	0.30	
L	0.51	0.61	0.71	
Dimensions in mm				

Figure 18 12DFN 6x7.7 Mechanical Outline